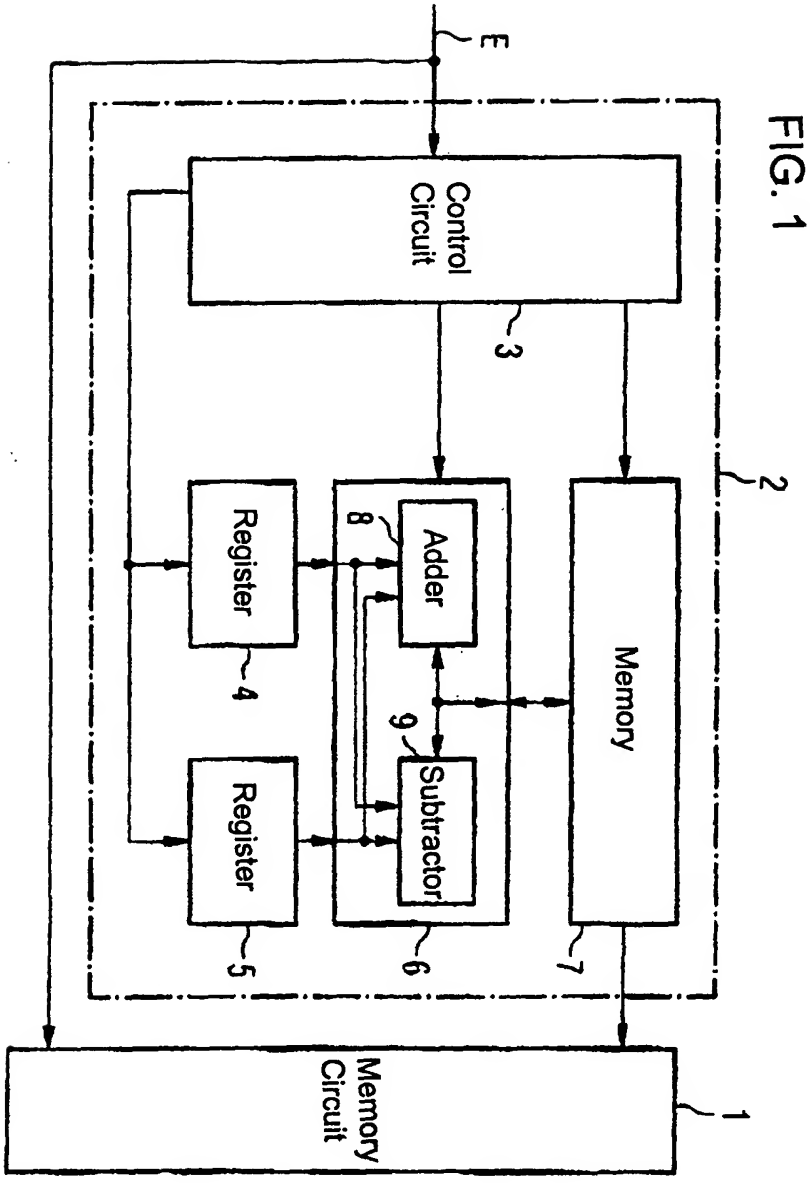
E
Control Circuit
3
2
Register
4
8
Adder
9
Subtractor
Register
5
6
Memory
7
Memory Circuit
1

FIG. 1

FIG. 2

Command/Pin	CLK	RAS	CAS	WE	CS	A10	A1	A0
READ	CLK	1	0	1	CS	0	ACTL	DCTL
READA	CLK	1	0	1	CS	1	ACTL	DCTL
WRITE	CLK	1	0	0	CS	0	ACTL	DCTL
WRITEA	CLK	1	0	0	CS	1	ACTL	DCTL
ACT	CLK	0	1	1	CS	x	ACTL	X
MRS	CLK	0	0	0	x	0	X	X
CBR	CLK	0	0	1	CS	x	x	x
PRE	CLK	0	1	0	CS	x	ACTL	x
NOP	CLK	1	1	1	1	1	1	X
NOP_A1	CLK	1	1	1	0	0	0	X
NOP_A2	CLK	1	1	1	0	1	0	X
NOP_S1	CLK	1	1	1	1	0	0	X
NOP_S2	CLK	1	1	1	1	1	0	X
NOP_Reset1	CLK	1	1	1	1	1	0	X
NOP_Reset2	CLK	1	1	1	1	1	1	x